**Hardik J Patel EEC 180A**

**Lab 5 Report – Latches, Flip-flops and Registers**

**July 15, 2015**

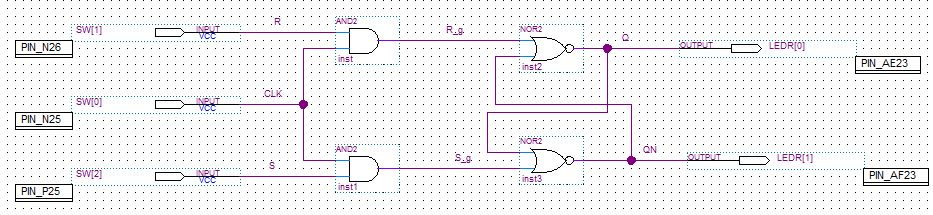
**Objective**

The purpose of this lab was to study the functionality and working of sequential logic design components, latches, flip-flops and registers. In this lab be design these components on the Quartus II software and then verify the designs on the DE2 board.

**Design and test procedure**

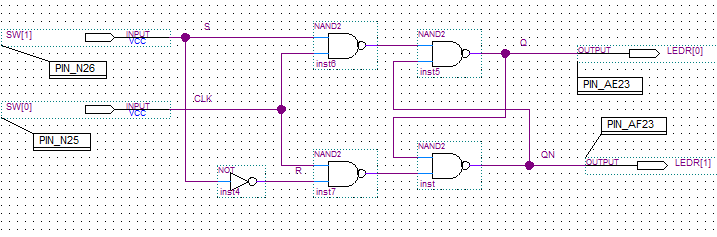
Part 1: For this part we implement the gated RS latch and study the inputs vs outputs of various combinations by verifying it on the DE2 board. This design uses cross-coupled NOR gates.

**Schematic of part 1 design:**

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Part 2: For this part we implemented the gated D latch, using only NAND gates and an inverter and studied the various outputs for different input combinations.

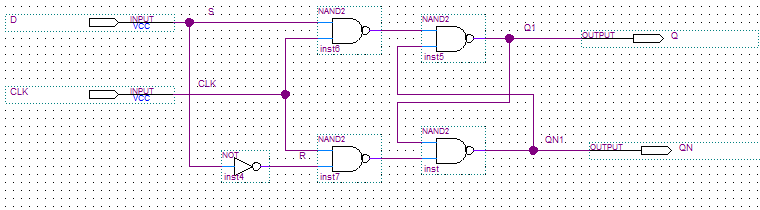
**Schematic of part 2 design:**

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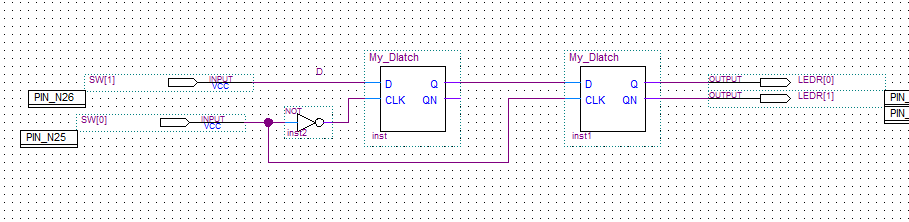
Part 3: In this part we implement an Edge Triggered D Flip-flop. For this we first create a symbol for the part 2 design of the gated D latch and then implement the latch in the master-slave configuration. Then we verify the design on the DE2 board.

**Schematic of part 3 design:**

Design for the My\_Dlatch symbol:

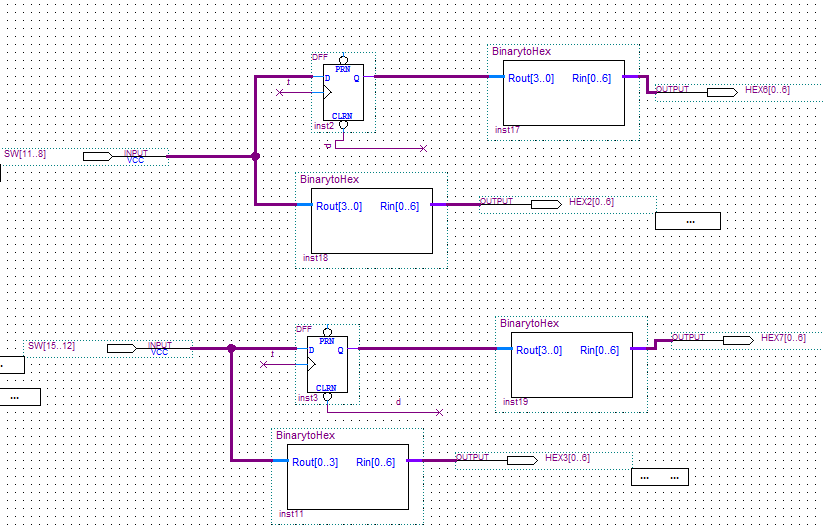
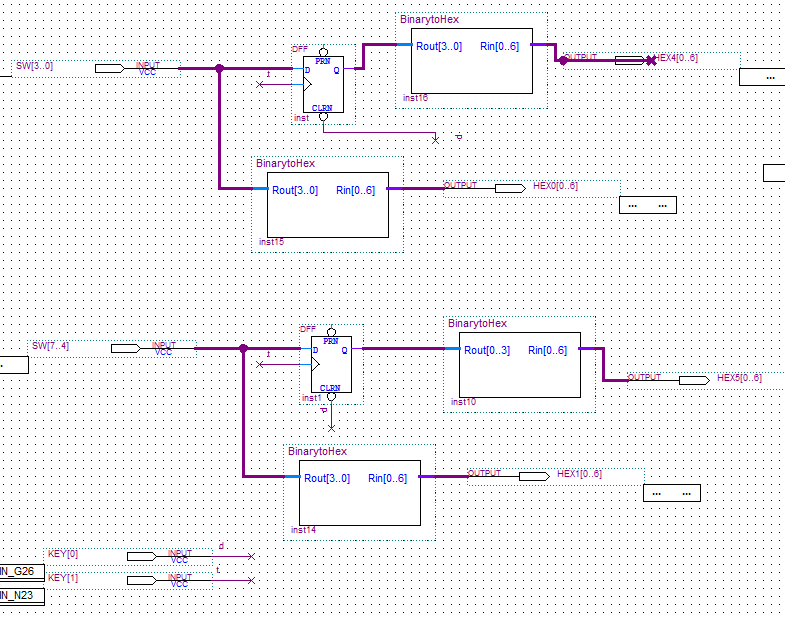


Design for the edge-triggered D flip-flop:

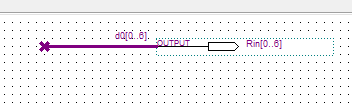
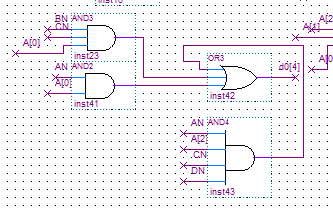
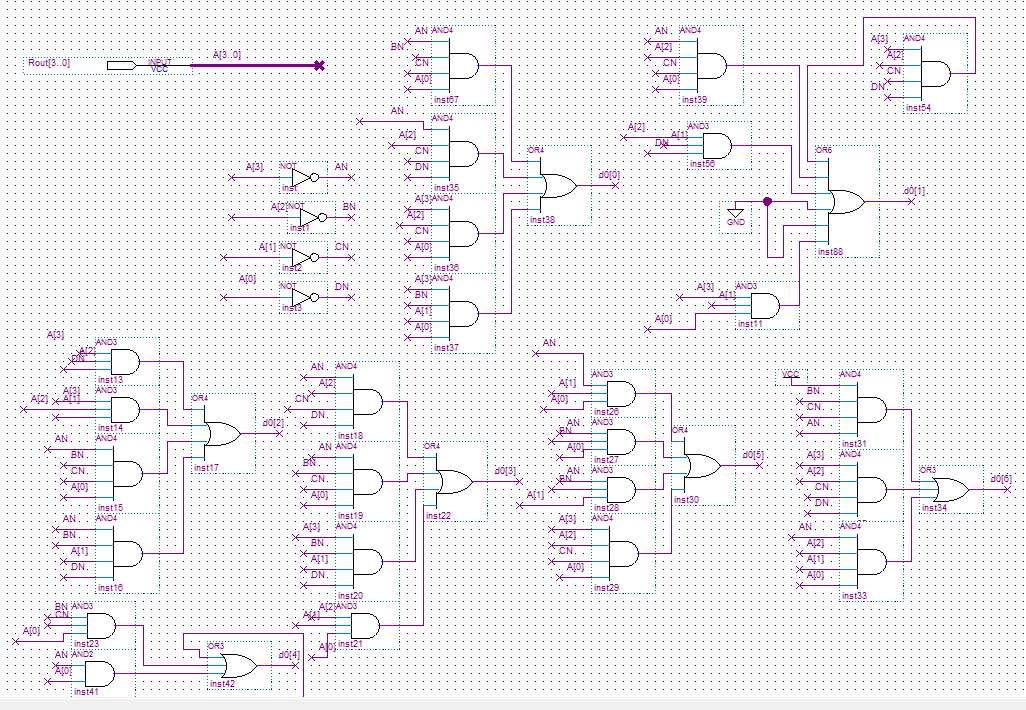


Part 4: For this part of the lab we built a 16 bit register and the output of the register is displayed in hexadecimal form by first building a design to convert binary to hexadecimal. For the binary to hex convertor we first find the sum of product equations for each segment of the display. This is done by first creating truth table determining which segments to turn off and which to turn on. Once the schematic was completed using 4 inputs, various NOT, AND and OR gates and 7 outputs, schematic was converted to a symbol for simplicity of the top level design. The inputs and output were also implemented using the bus feature for convenience. Then the schematic is implemented as shown below. This design takes four inputs in binary form and displays in hex and when the clock input falls to 0, the current values are stored, and displayed on hex4 to hex7.

**Schematic of part 4 design:**



**Schematic for the binary to hex convertor:**



**Results and Answers to Questions:**

Q1. When the CLK (SW[0]) is high, does the output change when R and S are changed? If so, give examples.

Ans. When clock high and RS turn from 01 to 10, the output changes from 1 to 0, since reset became high while set became 0.

Q2. When the CLK is low, does the output change when R and S are changed? If so, give examples.

Ans. When clock is low, the values of R\_g and S\_g will not change even if R and S change. This is due to the two and gated. Since, R\_g and S\_g do not change, the output will not change.

Q3. Is there any case when Q = QN? (i.e. when LEDR[1] and LEDR[0] are either both ON or both OFF). Describe this case. Since Q and QN should always be complements, this case would be an illegal state for an RS latch.

Ans. When the clock is high and R=S=1, this is when both NOR gates output zeroes, and hence the logic of Q = not QN breaks. Hence, this state should be illegal.

Q4. When R=S=0, what happens to the output when the CLK is toggled?

Ans. When R=S=0 and the clock is toggled, the outputs of R\_g and S\_g will remain 0, because of the two AND gates. In other word, when R=S=0, it doesn’t matter if the clock is toggled. Hence, the two outputs Q and QN will hold their values.

Q5. When R=S=1 and CLK goes from 1 to 0, what happens to the output? Explain why this happens. Is it what you expect?

Ans. In this case Q🡪1 and QN🡪0 and the system seems stable. This happens because S\_g becomes 0 and QN becomes 1, consequently, since R\_g is also 0, Q becomes 1. This is what is expected by looking at the design.

Q6. When CLK is high, does changing the D input affect the output? If so, give examples.

Ans. When clock is high and the input D changes from 0🡪1, the output resets and becomes 0. And when D changes from 1🡪0, the output sets and becomes 1.

Q7. When CLK is low, does changing the D input affect the output? If so, give examples.

Ans. When clock is low, D acts like a “don’t care” as Q and QN retain their previous values and the outputs do not change.

Q8. Is there any case when Q = QN? (i.e. when LEDR[1] and LEDR[0] are either both ON or both OFF). Describe this case. Since Q and QN should always be complements, this case would be an illegal state for a D latch.

Ans. Here there are not illegal cases and Q≠QN, for any combinations.

Q9. When CLK is high, does changing the D input affect the output? If so, give examples.

Ans. When the clock is high, changing D will not change the output.

Q10. When CLK is low, does changing the D input affect the output? If so, give examples.

Ans. When the clock is low, changing D will not change the output.

Q11. When does the output change? How is this different from a gated D latch?

Ans. Here the output only changes at an edge of a clock, i.e, when the clock rises the output and then the schematic will wait for another rise to change the output. This differs from the gated D latch as in the latch the output can change anytime the clock is high.

The results of part 4 were also expected as the register worked as it was supposed to.

**Conclusion:**

This this lab we leant and understood the working of latches, flip-flops and registers and understood their components and designs.